Features

- Single 2.5V or 2.7V to 3.6V Supply
- RapidS® Serial Interface: 66 MHz Maximum Clock Frequency
  - SPI Compatible Modes 0 and 3
- User Configurable Page Size
  - 256 Bytes per Page
  - 264 Bytes per Page
  - Page Size Can Be Factory Pre-configured for 256 Bytes
- Page Program Operation
  - Intelligent Programming Operation
  - 2,048 Pages (256/264 Bytes/Page) Main Memory
- Flexible Erase Options
  - Page Erase (256 Bytes)
  - Block Erase (2 Kbytes)
  - Sector Erase (64 Kbytes)
  - Chip Erase (4 Mbits)
- Two SRAM Data Buffers (256/264 Bytes)
  - Allows Receiving of Data while Reprogramming the Flash Array
- Continuous Read Capability through Entire Array
  - Ideal for Code Shadowing Applications
- Low-power Dissipation
  - 7 mA Active Read Current Typical
  - 25 µA Standby Current Typical
  - 5 µA Deep Power-down Typical
- Hardware and Software Data Protection Features
  - Individual Sector
- Sector Lockdown for Secure Code and Data Storage
  - Individual Sector
- Security: 128-byte Security Register
  - 64-byte User Programmable Space
  - Unique 64-byte Device Identifier
- JEDEC Standard Manufacturer and Device ID Read
- 100,000 Program/Erase Cycles Per Page Minimum
- Data Retention – 20 Years
- Industrial Temperature Range
- Green (Pb/Halide-free/RoHS Compliant) Packaging Options

4-megabit 2.5-volt or 2.7-volt DataFlash®

AT45DB041D

1. Description

The AT45DB041D is a 2.5V or 2.7V, serial-interface Flash memory ideally suited for a wide variety of digital voice-, image-, program code- and data-storage applications. The AT45DB041D supports RapidS serial interface for applications requiring very high speed operations. RapidS serial interface is SPI compatible for frequencies up to 66 MHz. Its 4,325,376 bits of memory are organized as 2,048 pages of 256 bytes or 264 bytes each. In addition to the main memory, the AT45DB041D also contains two SRAM buffers of 256/264 bytes each. The buffers allow the receiving of data while a page in the main Memory is being reprogrammed, as well as writing a continuous data stream. EEPROM emulation (bit or byte alterability) is easily handled with a self-contained three step read-modify-write operation. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the DataFlash uses a RapidS serial interface to sequentially access its data. The simple sequential access dramatically reduces active pin count, facilitates hardware layout,

increases system reliability, minimizes switching noise, and reduces package size. The device is optimized for use in many commercial and industrial applications where high-density, low-pin count, low-voltage and low-power are essential.

To allow for simple in-system reprogrammability, the AT45DB041D does not require high input voltages for programming. The device operates from a single power supply, 2.5V to 3.6V or 2.7V to 3.6V, for both the program and read operations. The AT45DB041D is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming and erase cycles are self-timed.

2. Pin Configurations and Pinouts

Table 2-1. Pin Configurations

Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	**Chip Select:** Asserting the $\overline{CS}$ pin selects the device. When the $\overline{CS}$ pin is deasserted, the device will be deselected and normally be placed in the standby mode (not Deep Power-Down mode), and the output pin (SO) will be in a high-impedance state. When the device is deselected, data will not be accepted on the input pin (SI). A high-to-low transition on the $\overline{CS}$ pin is required to start an operation, and a low-to-high transition is required to end an operation. When ending an internally self-timed operation such as a program or erase cycle, the device will not enter the standby mode until the completion of the operation.	Low	Input
SCK	**Serial Clock:** This pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command, address, and input data present on the SI pin is always latched on the rising edge of SCK, while output data on the SO pin is always clocked out on the falling edge of SCK.	–	Input
SI	**Serial Input:** The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched on the rising edge of SCK.	–	Input
SO	**Serial Output:** The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK.	–	Output
$\overline{WP}$	**Write Protect:** When the $\overline{WP}$ pin is asserted, all sectors specified for protection by the Sector Protection Register will be protected against program and erase operations regardless of whether the Enable Sector Protection command has been issued or not. The $\overline{WP}$ pin functions independently of the software controlled protection method. After the $\overline{WP}$ pin goes low, the content of the Sector Protection Register cannot be modified. If a program or erase command is issued to the device while the $\overline{WP}$ pin is asserted, the device will simply ignore the command and perform no operation. The device will return to the idle state once the $\overline{CS}$ pin has been deasserted. The Enable Sector Protection command and Sector Lockdown command, however, will be recognized by the device when the $\overline{WP}$ pin is asserted. The $\overline{WP}$ pin is internally pulled-high and may be left floating if hardware controlled protection will not be used. However, it is recommended that the $\overline{WP}$ pin also be externally connected to V_{CC} whenever possible.	Low	Input
RESET	**Reset:** A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level. The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. If this pin and feature are not utilized it is recommended that the $\overline{RESET}$ pin be driven high externally.	Low	Input
V_{CC}	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	–	Power
GND	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.	–	Ground

18. Electrical Specifications

Table 18-1. Absolute Maximum Ratings*

Temperature under Bias	-55° C to +125° C
Storage Temperature	-65° C to +150° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 18-2. DC and AC Operating Range

		AT45DB041D (2.5V Version)	AT45DB041D
Operating Temperature (Case)	Ind.	-40° C to 85° C	-40° C to 85° C
V_{CC} Power Supply		2.5V to 3.6V	2.7V to 3.6V

Table 18-3. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DP}	Deep Power-down Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		5	10	µA
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		25	50	µA
I_{CC1} (1)	Active Current, Read Operation	f = 20 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		7	10	mA
		f = 33 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		8	12	mA
		f = 50 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		10	14	mA
		f = 66 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		11	15	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		12	17	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input Low Voltage				V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

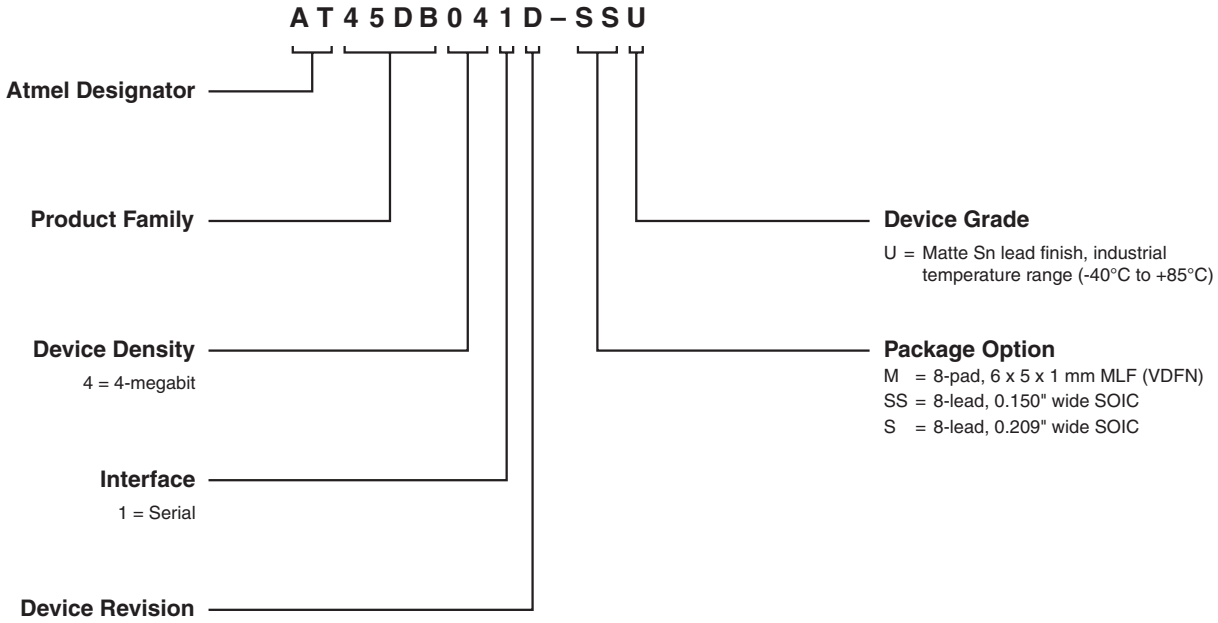
Notes: 1. I_{CC1} during a buffer read is 20 mA maximum @ 20 MHz.
2. All inputs are 5 volts tolerant.

Table 18-4. AC Characteristics – RapidS/Serial Interface

Symbol	Parameter	AT45DB041D (2.5V Version)			AT45DB041D			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK}	SCK Frequency			50			66	MHz
f_{CAR1}	SCK Frequency for Continuous Array Read			50			66	MHz
f_{CAR2}	SCK Frequency for Continuous Array Read (Low Frequency)			33			33	MHz
t_{WH}	SCK High Time	6.8			6.8			ns
t_{WL}	SCK Low Time	6.8			6.8			ns
t_{SCKR}[1]	SCK Rise Time, Peak-to-Peak (Slew Rate)	0.1			0.1			V/ns
t_{SCKF}[1]	SCK Fall Time, Peak-to-Peak (Slew Rate)	0.1			0.1			V/ns
t_{CS}	Minimum $\overline{CS}$ High Time	50			50			ns
t_{CSS}	$\overline{CS}$ Setup Time	5			5			ns
t_{CSH}	$\overline{CS}$ Hold Time	5			5			ns
t_{SU}	Data In Setup Time	2			2			ns
t_{H}	Data In Hold Time	3			3			ns
t_{HO}	Output Hold Time	0			0			ns
t_{DIS}	Output Disable Time			8			6	ns
t_{V}	Output Valid			8			6	ns
t_{WPE}	$\overline{WP}$ Low to Protection Enabled			1			1	µs
t_{WPD}	$\overline{WP}$ High to Protection Disabled			1			1	µs
t_{EDPD}	$\overline{CS}$ High to Deep Power-down Mode			3			3	µs
t_{RDPD}	$\overline{CS}$ High to Standby Mode			35			35	µs
t_{XFR}	Page to Buffer Transfer Time			200			200	µs
t_{comp}	Page to Buffer Compare Time			200			200	µs
t_{EP}	Page Erase and Programming Time (256/264 bytes)		14	35		14	35	ms
t_{P}	Page Programming Time (256/264 bytes)		2	4		2	4	ms
t_{PE}	Page Erase Time (256/264 bytes)		13	32		13	32	ms
t_{BE}	Block Erase Time (2,048/2,112 bytes)		30	75		30	75	ms
t_{SE}	Sector Erase Time (65,536/67,584 bytes)		1.6	5		1.6	5	s
t_{CE}	Chip Erase Time		6	12		6	12	s
t_{RST}	$\overline{RESET}$ Pulse Width	10			10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1			1	µs

26. Ordering Information

26.1 Ordering Code Detail



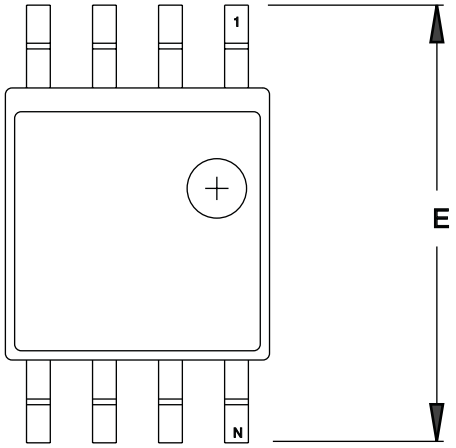
26.2 Green Package Options (Pb/Halide-free/RoHS Compliant)

Ordering Code[1][2]	Package	Lead Finish	Operating Voltage	f_{SCK} (MHz)	Operation Range
AT45DB041D-MU AT45DB041D-MU-SL954[3] AT45DB041D-MU-SL955[4]	8M1-A	Matte Sn	2.7V to 3.6V	66	Industrial (-40°C to +85°C)
AT45DB041D-SSU AT45DB041D-SSU-SL954[3] AT45DB041D-SSU-SL955[4]	8S1				
AT45DB041D-SU AT45DB041D-SU-SL954[3] AT45DB041D-SU-SL955[4]	8S2				
AT45DB041D-MU-2.5	8M1-A	Matte Sn	25V to 3.6V	50	
AT45DB041D-SSU-2.5	8S1				
AT45DB041D-SU-2.5	8S2				

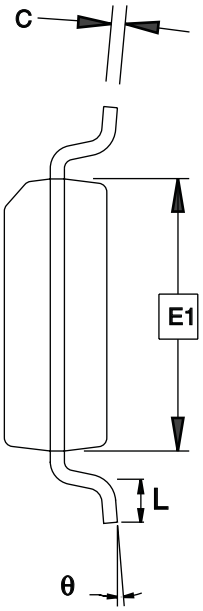
Notes:
1. The shipping carrier option is not marked on the devices.
2. Standard parts are shipped with the page size set to 264 bytes. The user is able to configure these parts to a 256-byte page size if desired.
3. Parts ordered with suffix SL954 are shipped in bulk with the page size set to 256 bytes. Parts will have a 954 or SL954 marked on them.
4. Parts ordered with suffix SL955 are shipped in tape and reel with the page size set to 256 bytes. Parts will have a 954 or SL954 marked on them.

Package Type	
8M1-A	8-pad, 6 x 5 x 1.00 mm Body, Very Thin Dual Flat Package No Lead MLF™ (VDFN)
8S1	8-lead, 0.150” Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8S2	8-lead, 0.209” Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)

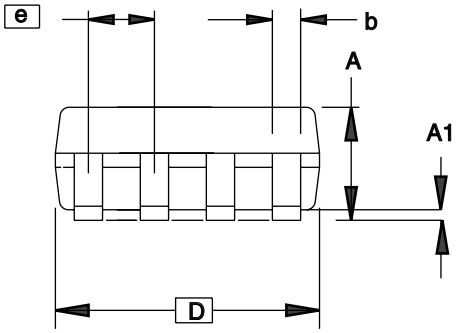
27.3 8S2 – EIAJ SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	5
C	0.15		0.35	5
D	5.13		5.35	
E1	5.18		5.40	2, 3
E	7.70		8.26	
L	0.51		0.85	
θ	0°		8°	
e	1.27 BSC			4

Notes:
1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs are not included.
3. It is recommended that upper and lower cavities be equal. If they are different, the larger dimension shall be regarded.
4. Determines the true geometric position.
5. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8S2**, 8-lead, 0.209" Body, Plastic Small Outline Package (EIAJ)	8S2	D